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(54) Semiconductor device having a trench for device isolation and method of fabricating the same.

(57) A device-isolating trench (28) having a taper at its upper portion is formed in a silicon semiconductor substrate (22). Then, a silicon oxide film (32) is formed on the inner wall of the trench (28) and the surface of the semiconductor substrate (22) near the trench (28) by an oxidizing method, and polycrystalline silicon (33) is buried in the trench (28).

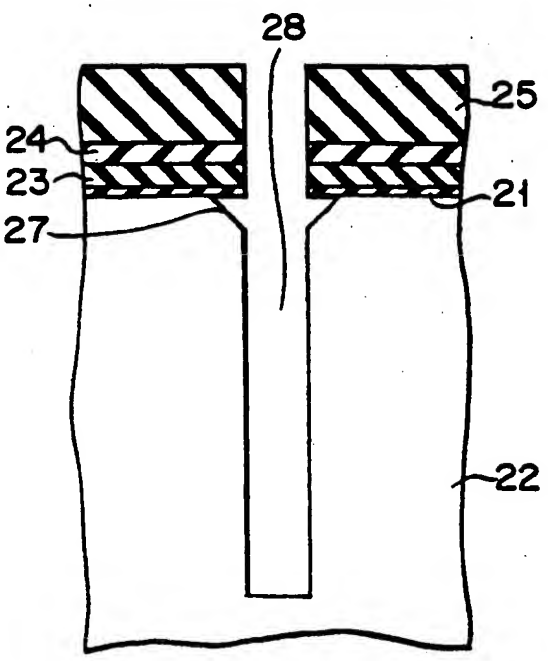

FIG. 2C

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The present invention relates to a semiconductor device in which device isolation is made by a trench formed in a semiconductor substrate, and a method of fabricating the same.

Conventionally, device isolation using such a trench is carried out in the following manner.

As shown in Fig. 1A, a trench 11 is formed in a semiconductor substrate 12, and a thin oxide film 13 is formed on the inner wall of the trench 11. A nonoxide film 14 is then formed only on a device region 15.

Then, with the nonoxide film 14 used as a mask, the resultant structure is subjected to an oxidization treatment to form a thick oxide film 16 on the surface of the device region 15 except on a part thereof, as shown in Fig. 1B.

Thereafter, polycrystalline silicon is buried in the trench 11 where the oxide film 16 is formed, followed by flattening of the top surface of the polycrystalline silicon, deposition of a cap oxide film, and so forth, thereby providing the device isolation.

According to this conventional method, the wall of the trench 11 and the surface of the substrate 12 define almost right angles at an upper corner portion 17 of the trench 11, as shown in Fig. 1B. At the time the thick oxide film 16 is formed, therefore, thermal stress is concentrated on the corner portion 17 at the oxidization time, or so is stress originated from expansion of volume or the like. This causes dislocation in the oxide film 16 near the corner portion.

This dislocation impairs the device isolation characteristic and the characteristic of a device formed in the device region. For instance, if bipolar transistors are respectively formed in multiple device regions, the dislocation results in an increase in leak current between the collectors of the individual transistors and deterioration of the current amplification factor. In other words, since the presence of dislocation to a certain degree increases the recombination current, the device characteristic and the device isolation characteristic are deteriorated.

It is therefore an object of the present invention to provide a semiconductor device, which can suppress the occurrence of dislocation in an oxide film at the upper corner portion of a trench for device isolation and can thus improve the characteristic of a device formed in a device region as well as the device isolation characteristic, and a method of fabricating the same.

According to one aspect of the present invention, there is provided a method of fabricating a semiconductor device, which comprises a first step of forming a device-isolating trench with a taper at an upper portion thereof, in a semiconductor substrate; and a second step of forming an oxide film on an inner wall of the trench and a surface of the semiconductor substrate near the trench by an oxidizing method.

According to another aspect of the present invention, there is provided a semiconductor device comprising a semiconductor substrate; a device-isolating trench formed in the semiconductor substrate; and an insulating film so formed as to cover an inner wall of the trench and a surface of the semiconductor substrate near the trench, with a radius of curvature of 0.1 μm or greater at an upper corner portion of the trench.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A and 1B are cross-sectional views of individual steps of a conventional method of fabricating a semiconductor device;

Figs. 2A to 2H are cross-sectional views of individual steps of a conventional method of fabricating a semiconductor device according to the first embodiment of the present invention;

Fig. 3 is a perspective view illustrating the structure of a bipolar transistor fabricated by th method according to the first embodiment;

Figs. 4A to 4E are cross-sectional views of individual steps of a conventional method f fabricating a semiconductor device according to the second embodiment of the present invention; and

Fig. 5 is a diagram illustrating the characteristic of the semiconductor devices fabricated by the methods according to the first and second embodiments.

Preferred embodiments of the present invention will now be described referring to the accompanying drawings.

First, a silicon oxide film 21 is formed on th whole surface of a silicon semiconductor substrate 22 by a thermal oxidizing method, and a silicon nitride film 23 is then formed on the oxide film 21, as shown in Fig. 2A. Subsequently, a silicon oxide film 24 is deposited on the silicon nitride film 23 by a CVD (Chemical Vapor Deposition) method, followed by coating of a photoresist on the entire surface of the resultant structure. The photoresist is then subjected to pattern exposure and developing processing, thus forming photoresist mask 25.

Next, by using an isotropic etching method, such as RIE (Reactive Ion Etching), with the mask 25, the silicon oxide film 24 and silicon nitride film 23 are selectively removed. Subsequently, by using an isotropic etching method, such as a wet etching method involving a mixture of a hydrofluric acid and a nitric acid, the underlying substrate 22 is further removed about 0.5 μm, forming a trench 26 in the substrate 22. It is to be noted that, as the

isotropic etching method, a plasma etching method called "CDE (Chemical Dry Etching)" may replace the wet etching method.

Th n, by using th isotropic etching method, such as a wet etching method involving a mixture of isopropyl alcohol, KOH and water, with the mask 25, the substrate 22 at the upper portion of the trench 26 is etched, forming a taper portion 27 in the substrate 22, as shown in Fig. 2B.

Next, the trench 26 is further etched by anisotropic etching, such as RIE, thereby forming a trench 28, 5 to 7 μm deep, as shown in Fig. 2C.

Fig. 2D illustrates multiple trenches 28 formed through the above-described individual steps. These trenches 28 isolate individual device regions 29 from one another.

Then, after the resist mask 25, silicon oxide film 24, silicon nitride film 23 and silicon oxide film 21 are removed, the resultant structure is subjected to thermal oxidization at 950° C in the environment of a gas mixture of H_2 and O_2, forming a silicon oxide film 30 having a thickness of about 0.05 μm on the surface of the semiconductor substrate 22 and the inner wall of the trench 28, as shown in Fig. 2E. Subsequently, a silicon nitride film 31 is deposited 0.05 to 0.15 μm thick on the entire surface of the resultant structure at 780° C by a low pressure CVD method. The silicon nitride film 31 is selectively etched to remain on each device region 29 by a plasma etching method. The remaining silicon nitride film 31 is to be used as a nonoxide film in the subsequent step.

Next, as shown in Fig. 2F, by a wet oxidizing method using the nonoxide film (silicon nitride film 31) as an oxidization-resistant mask, a silicon oxide film 32 is formed about 0.8 μm thick on part of each device region 29 where the silicon nitride film 31 is not formed, and the inner wall of each trench 28. Fig. 2G presents an enlarged illustration of one of the trenches after the above step has been completed.

Then, after the silicon nitride film 31 is removed, polycrystalline silicon 33 is buried in each trench 28 and its surface is flattened, followed by formation of a thin cap oxide film 34 on the trench 28, as shown in Fig. 2H.

Thereafter, a bipolar transistor having, for example, an N type emitter region E, a P type base region B and an N type collector region C, is formed in each device region 29 by a known method, as shown in Fig. 3. Referring to Fig. 3, the substrate 22 has a three-layer structure including a P type region 41, an N^+ type buried region 42 and an N type epitaxial region 43. It is to be noted that a P^+ type region 44 is formed in the bottom of each trench 28 by an ion implantation method or diffusion method before the polycrystalline silicon 33 is buried therein.

According to the method of the first embodiment, the tap r portion 27 is formed in the substrate 22 at the upper portion of the trench 28 at th time the step illustrated in Fig. 2B is ex cut d, and the resultant structure is subjected to oxidization in the subsequent step, thereby forming the silicon oxide film 32. In forming the silicon oxide film 32, therefore, an upper corner portion of the trench 28 will be shaped round with some radius of curvature, not square, as shown in Fig. 2G.

It is therefore possible to relax the concentration of thermal stress on the corner portion at the oxidization time, or the concentration of stress originated from expansion of volume or the like thereon. This suppresses the occurrence of dislocation near the corner portion of the trench, which has been a bottleneck in the prior art, thus ensuring improvement of the device isolation characteristic and the characteristic of a device formed in each device region.

A method according to the second embodiment of the present invention will be described below referring to Figs. 4A to 4E.

First, as in the case illustrated in Fig. 4A, a silicon oxide film 21 is formed on the whole surface of a silicon semiconductor substrate 22 by a thermal oxidizing method, and a silicon nitride film 23 is then formed on the oxide film 21. Subsequently, a silicon oxide film 24 is deposited on the silicon nitride film 23 by a CVD method, followed by coating of a photoresist on the entire surface of the resultant structure. The photoresist is then subjected to pattern exposure and developing processing, thus forming photoresist mask 25. Then, by using an anisotropic etching method, such as RIE, with the mask 25, the silicon oxide film 24, silicon nitride film 23 and silicon oxide film 21 are selectively removed, forming an opening 35.

Next, a trench 28 is formed 5 to 7 μm deep in the substrate 22 by the RIE using the mask 25, as shown in Fig. 4B. This trench isolates the device regions from each other as in the case shown in Fig. 2D. At the time the etching is performed, a polymer 36 is adhered as a reaction product to the side wall of the trench 28.

Then, as shown in Fig. 4C, the polymer 36 adhered to the side wall of the trench 28 is removed by a wet etching method. At the same time, the entire silicon oxide film 24 is removed. That part of the silicon oxide film 21 which is adjacent to the trench 28 is also removed. Then, the substrate 22 at the upper portion of the trench 28 is etched using the CDE, thereby forming a taper portion 27 in the substrate 22. At the same time, the bottom of the trench 28 is etched, rounding its bottom edge portions.

Then, as shown in Fig. 4D, after the silicon nitride film 23 and silicon oxide film 21 are re-

moved, the resultant structure is subjected to thermal oxidization at 950° C in the environment of a gas mixture of H_2 and O_2, forming a silicon oxide film 30 having a thickness of about 0.05 μm on the surface of the semiconductor substrate 22 and the inner wall of the trench 28, as per the first embodiment. Subsequently, a silicon nitride film 31 is deposited 0.05 to 0.15 μm thick on the entire surface of the resultant structure at 780° C by a low pressure CVD method. The silicon nitride film 31 is selectively etched to remain on a device region 29 by a plasma etching method. Then, by a wet oxidizing method using the silicon nitride film 31 as an oxidization-resistant mask, a silicon oxide film 32 is formed 0.8 μm thick on part of the device region 29 where the silicon nitride film 31 is not formed, and the inner wall of each trench 28. At this time, as illustrated, the upper corner portion of the trench 28 will be shaped round with some radius of curvature, R, not square. The oxidization is executed so that the radius of curvature, R, becomes about 0.1 μm.

Then, after the silicon nitride film 31 is removed, polycrystalline silicon 33 is buried in the trench 28 and its surface is flattened, followed by formation of a thin cap oxide film 34 on the trench 28, as shown in Fig. 4E.

Thereafter, a bipolar transistor having an emitter region E, a base region B and a collector region C, is formed in each device region 28 by a known method, as shown in Fig. 3, as per the first embodiment.

According to the method of the second embodiment too, the taper portion 27 is formed in the substrate 22 at the upper portion of the trench 28 at the time the step illustrated in Fig. 4C is executed, and the resultant structure is subjected to oxidization in the subsequent step, thereby forming the silicon oxide film 32. In forming the silicon oxide film 32, therefore, the upper corner portion of the trench 28 will be shaped round with a radius of curvature of about 0.1 μm, not square, as shown in Fig. 4D.

In the second embodiment, therefore, it is possible to relax the concentration of thermal stress on the corner portion at the oxidization time, or the concentration of stress originated from expansion of volume or the like thereon. This suppresses the occurrence of dislocation near the corner portion of the trench, which has been a bottleneck in the prior art, thus ensuring improvement of the device isolation characteristic and the characteristic of a device form d in each devic region.

Fig. 5 is a characteristic diagram illustrating the relationship between the radius of curvature, R, at the upper corner portion of the trench 28 and the dislocation density when bipolar transistors are formed in the device regions of the semiconductor substrate isolated by the methods of the first and second embodiments. As illustrated, with the radius of curvature, R, set 0.1 μm or larger, the dislocation can be suppressed as compared with the prior art in which R is almost 0. As a result, the devic isolation characteristic and the characteristic of devices formed in the device regions can be improved. The radius of curvature, R, at the upper corner portion of the trench 28 is not limited to about 0.1 μm, but can be set larger. It is to be noted that the larger the radius of curvature, R, the greater the effect of suppressing the dislocation.

Claims

1. A method of fabricating a semiconductor device comprising:
   a first step of forming a device-isolating trench with a taper at an upper portion thereof, in a semiconductor substrate; and
   a second step of forming an oxide film on an inner wall of said trench and a surface f said semiconductor substrate near said trench by an oxidizing method.

2. A method according to claim 1, characterized by further comprising a third step of burying polycrystalline silicon in said trench.

3. A method according to claim 1, characterized in that said first step includes:
   a fourth step of etching said semiconductor substrate to form a shallow trench;
   a fifth step of etching said semiconductor substrate at an upper corner portion of said shallow trench in a taper shape; and
   a sixth step of further etching said semiconductor substrate to make a deep trench out of said shallow trench.

4. A method according to claim 3, characterized in that with the depth of said shallow trench formed in said fourth step being 1, said d p trench is formed 10 times as deep as said shallow trench or deeper in said sixth step.

5. A method according to claim 3, characterized in that said shallow trench is formed 0.5 μm deep or shallower in said fourth step.

6. A method according to claim 3, characterized in that said deep trench is formed 5 μm deep or deeper in said sixth step.

7. A method according to claim 3, characterized in that said fourth step is performed by an isotropic etching.

8. A method according to claim 3, characterized in that said fifth step is performed by wet etching.

9. A method according to claim 3, characterized in that said sixth step is performed by anisotropic etching.

10. A method according to claim 1, characterized in that said first step includes:

a seventh step of etching said semiconductor substrate to form a deep trench; and

an eighth step of etching said semiconductor substrate at an upper corner portion of said deep trench in a taper shape.

11. A method according to claim 10, characterized in that said seventh step is performed by anisotropic etching.

12. A method according to claim 10, characterized in that said eighth step is performed by isotropic etching.

13. A semiconductor device comprising:

a semiconductor substrate;

a device-isolating trench formed in said semiconductor substrate; and

an insulating film so formed as to cover an inner wall of said trench and a surface of said semiconductor substrate near said trench, with a radius of curvature of 0.1 μm or greater at an upper corner portion of said trench.

14. A semiconductor device according to claim 13, characterized in that said insulating film has a thickness of about 0.8 μm.

15. A semiconductor device according to claim 13, characterized in that a bipolar transistor is formed in a device region isolated by said device-isolating trench.

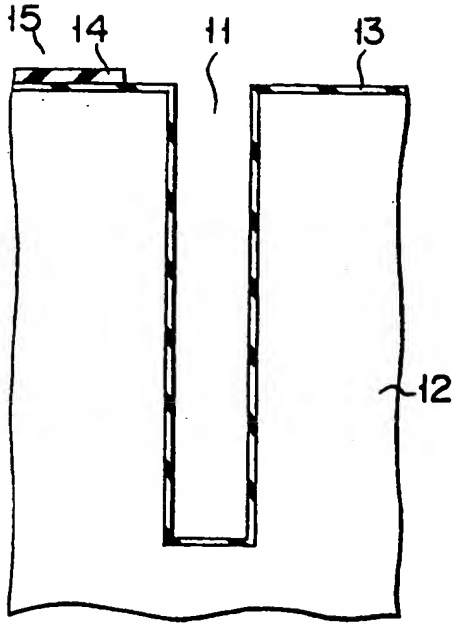

FIG. 1A

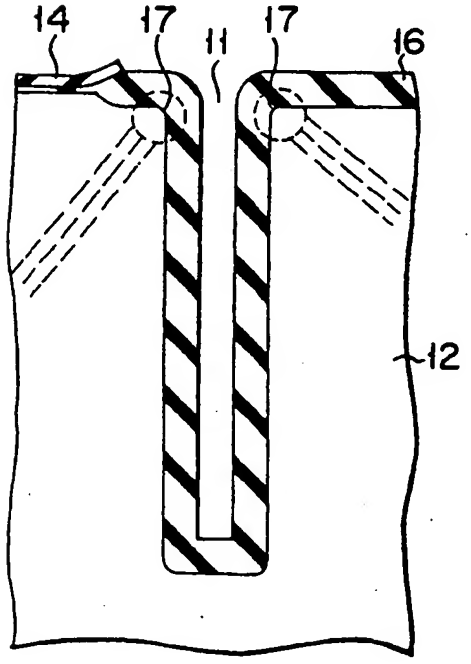

FIG. 1B

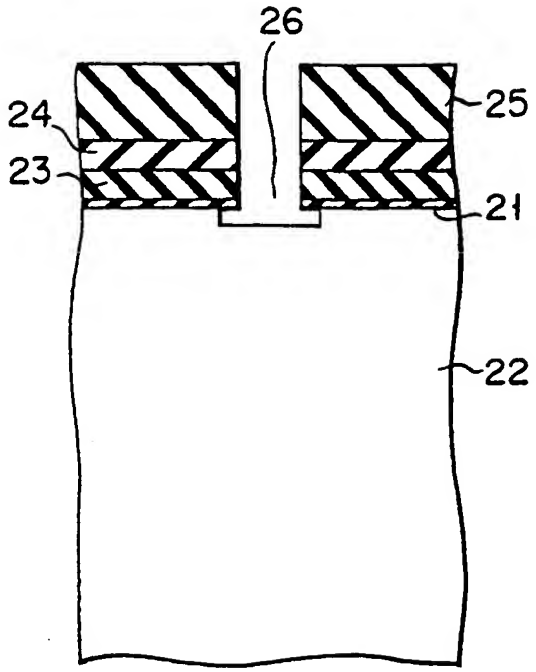

FIG. 2A

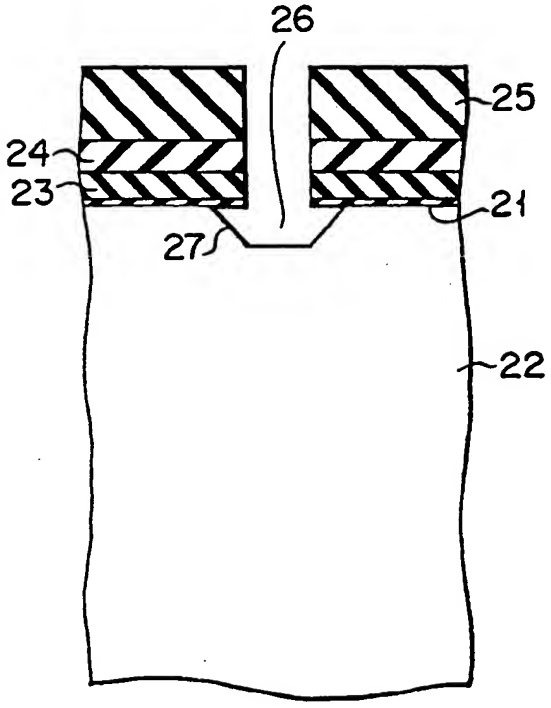

FIG. 2B

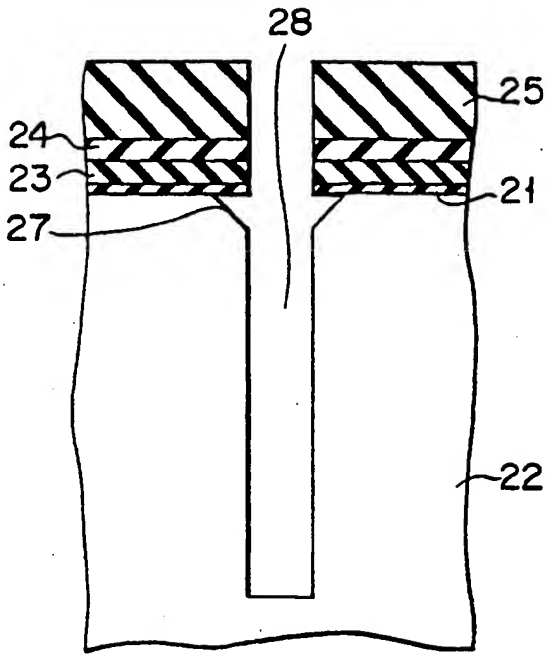

FIG. 2C

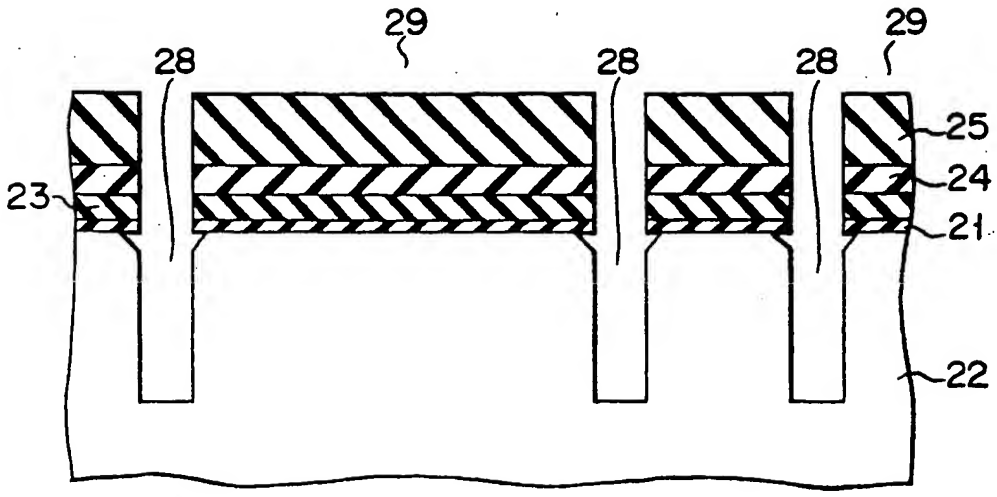

FIG. 2D

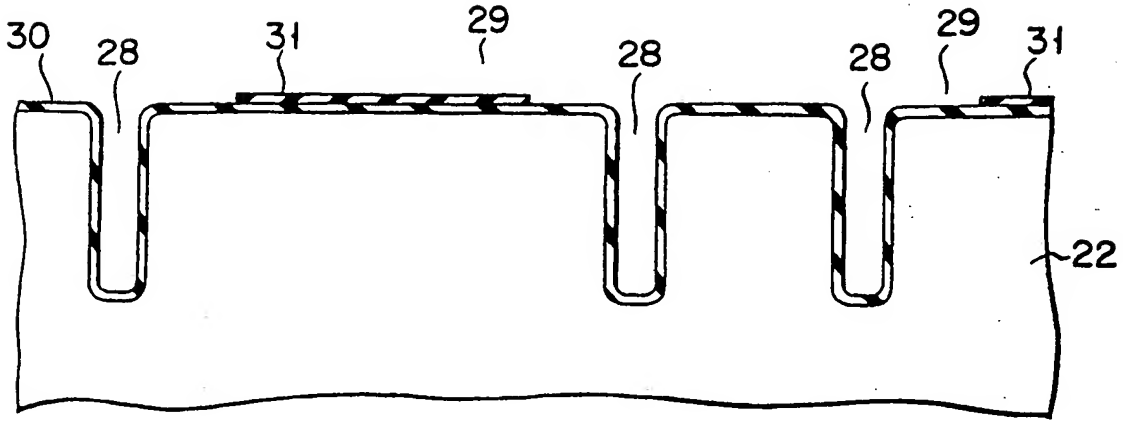

FIG. 2E

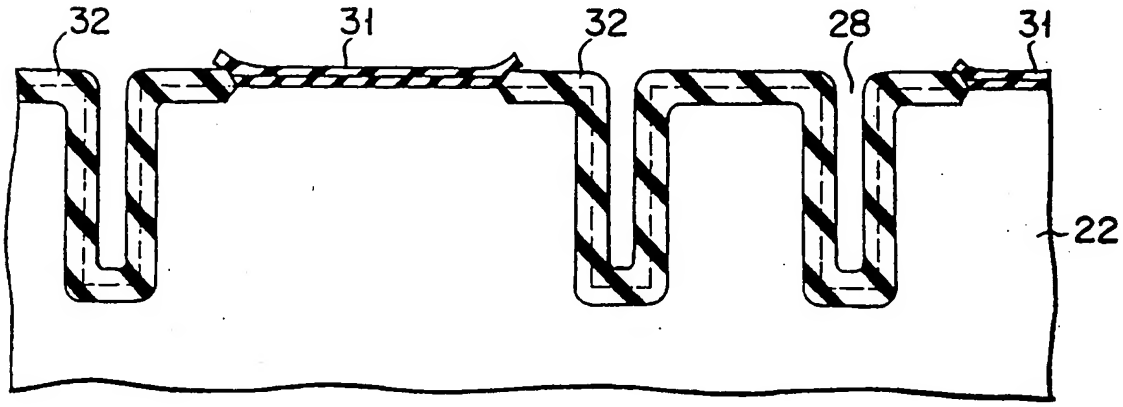

FIG. 2F

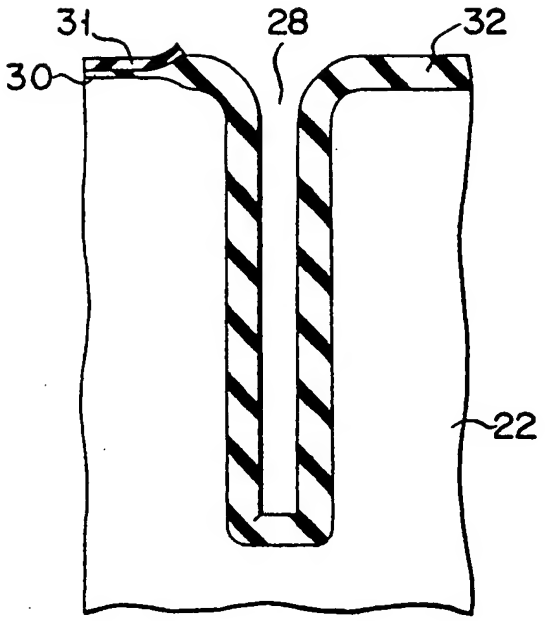

FIG. 2G

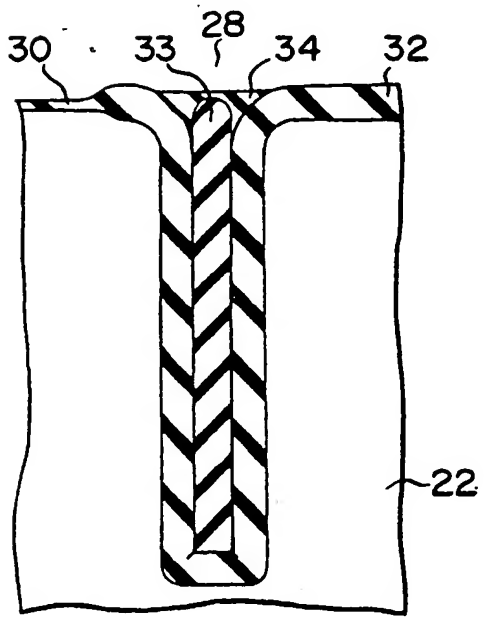

FIG. 2H

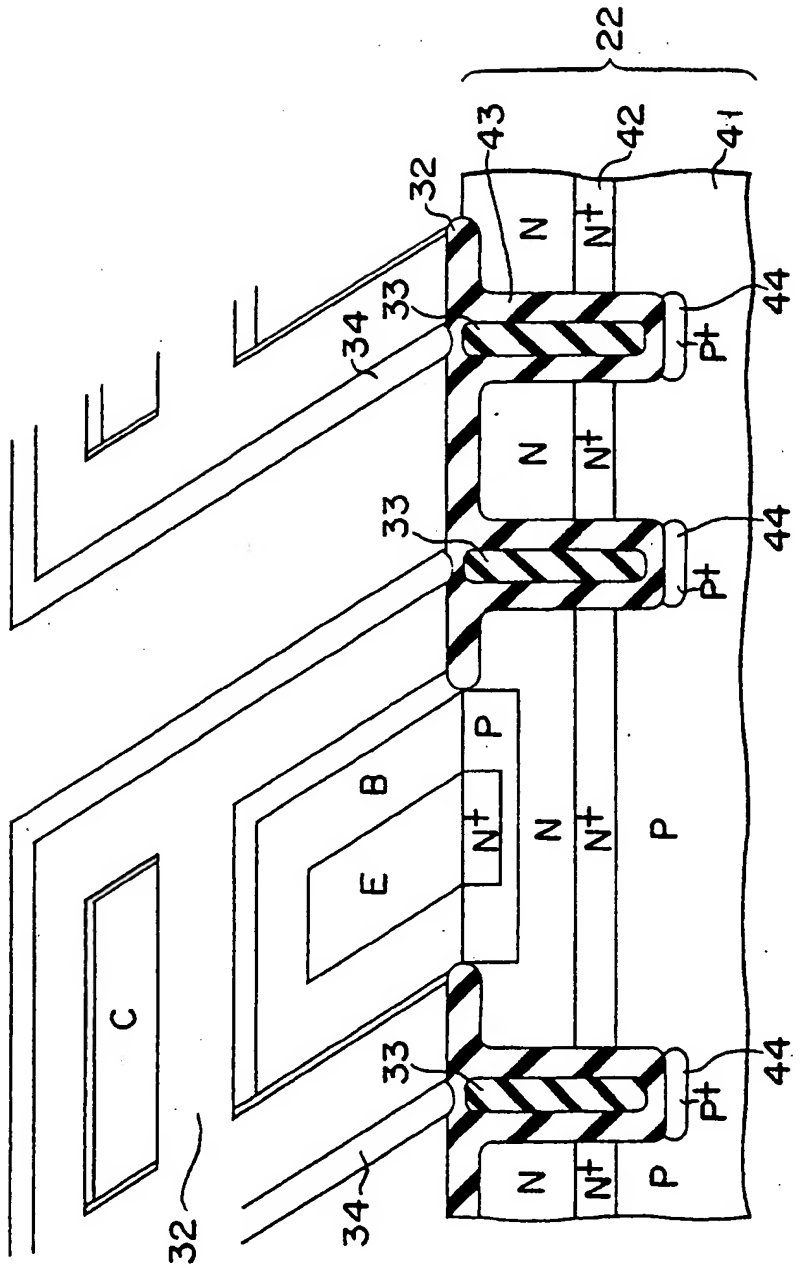

FIG. 3

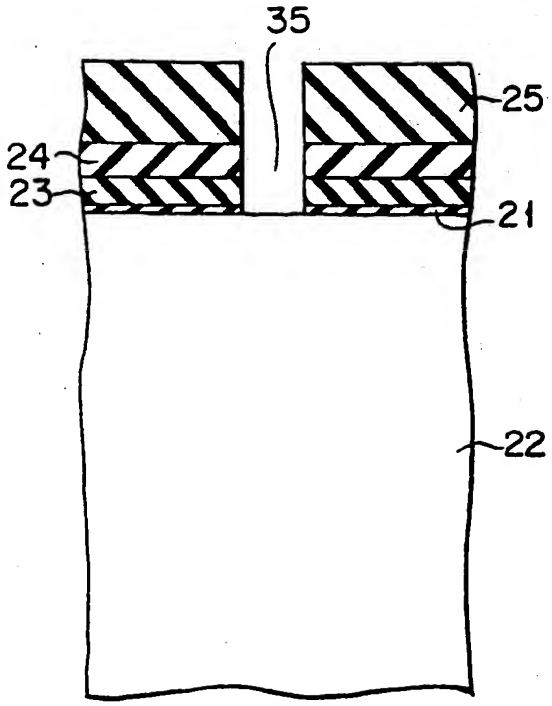

FIG. 4A

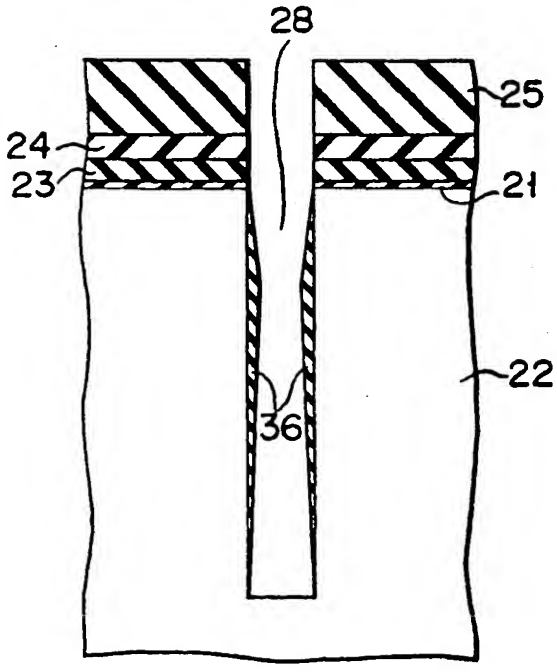

FIG. 4B

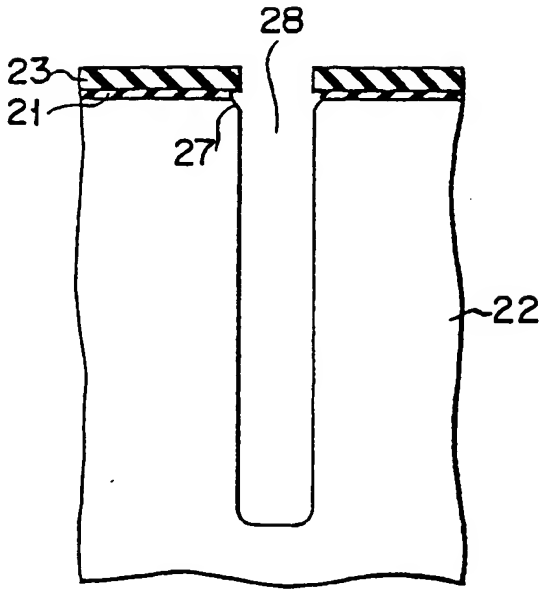

FIG. 4C

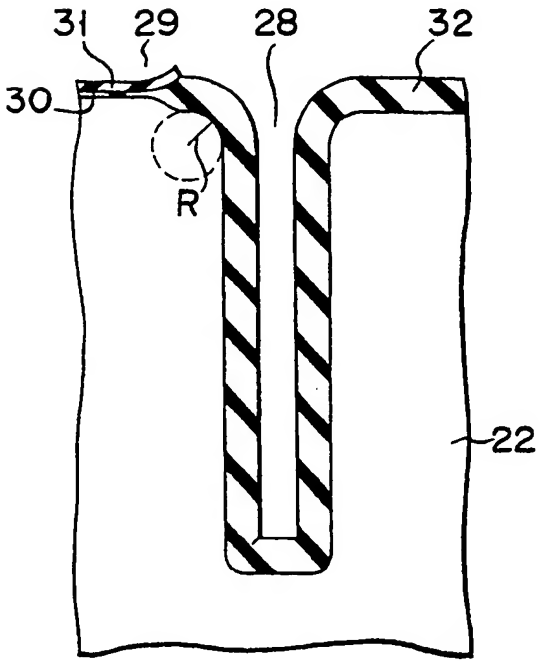

FIG. 4D

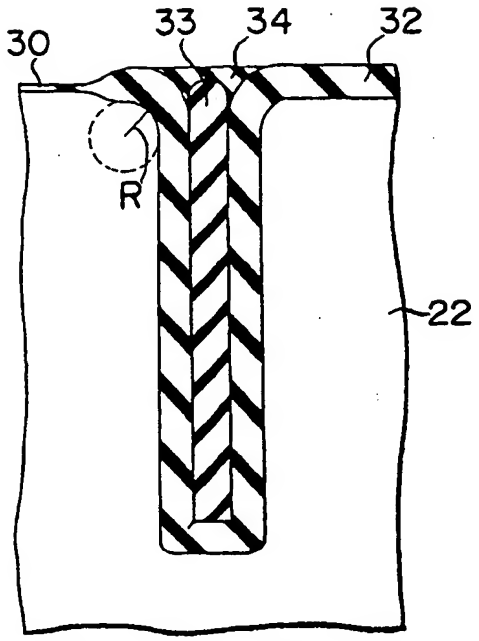
30
33
34
32
R
22

FIG. 4E

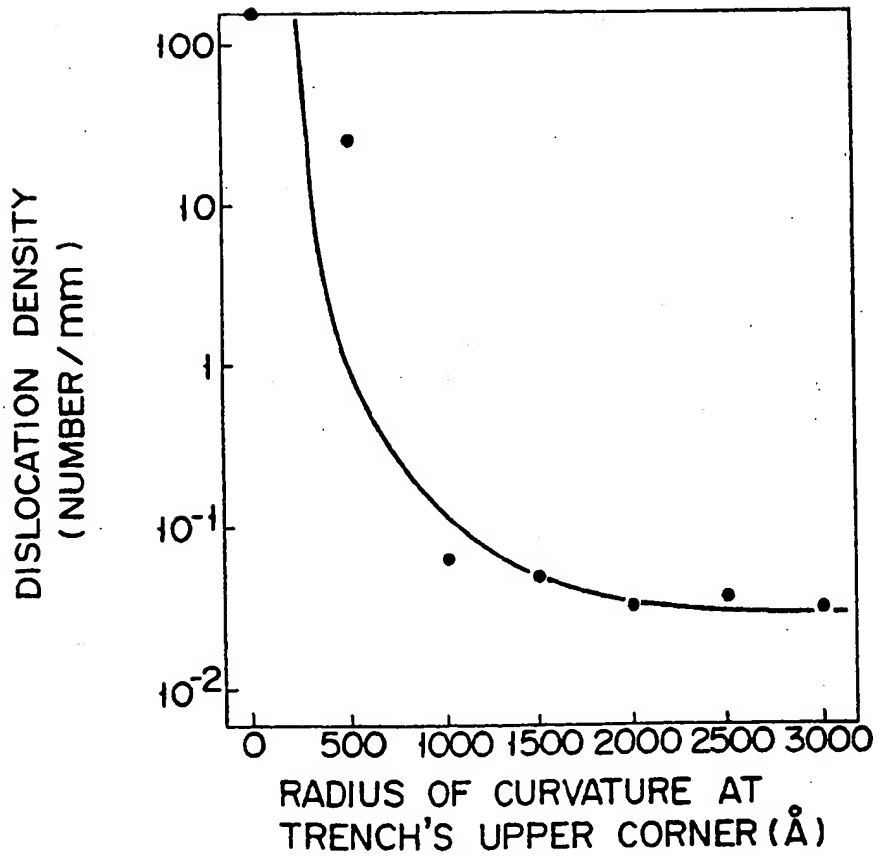
DISLOCATION DENSITY
(NUMBER/mm)
100
10
1
10-1
10-2
0
500
1000
1500
2000
2500
3000
RADIUS OF CURVATURE AT
TRENCH'S UPPER CORNER (Å)

FIG. 5

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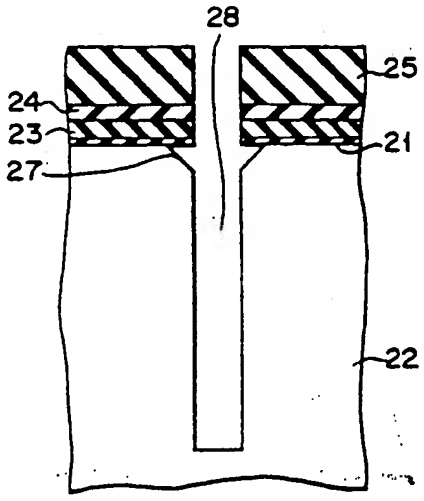

FIG. 2C

EP 0 459 397 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 91 10 8691

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol.135, no.3, March 1988, MANCHESTER, NEW HAMPSHIRE US pages 726 - 730 Y. TAMAKI ET AL. 'EVALUATION OF DISLOCATION GENERATION IN U-GROOVE ISOLATION.' * the whole document * ---	1	H01L21/76 H01L21/308
X	IEDM -DECEMBER 13-14-15,1982, 1982, NEW-YORK pages 62 - 65 A. HAYASAKA ET AL. 'U-GROOVE ISIOLATION TECHNIQUE FOR HIGH SPEED BIPOLAR VLSI'S' * the whole document * * figure 4 * ---	1,2 15	
X	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol.134, no.2, February 1987, MANCHESTER, NEW HAMPSHIRE US pages 481 - 490 L. O. WILSON 'OXIDATION OF CURVED SILICON SURFACES' * page 481, left column, paragraph 1 - page 482, left column, paragraph 2; figures 2-9,A-1-B4 * ---	13,14	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A	JAPANESE JOURNAL OF APPLIED PHYSICS, SUPPLEMENTS 18TH CONFERENCE ON SOLID STATE DEVICES AUGUST 20-22 1986, 1986, TOKYO JA pages 303 - 306 K. IMAI ET AL. 'DECREASE IN TRENCHED SURFACE OXIDE LEAKAGE CURRENTS BY ROUNDING OFF OXIDATION' * the whole document * -----	13,14	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	22 June 1994	VANCRAEYNEST, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EP 9110 8691.6

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.

namely:

See Sheet B.

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: 1-2, 13-14

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

Claims 1-2, 13-15: Method for forming a trench isolation region provided with an oxide layer and filling said trench with polysilicon. Semiconductor device with trench isolation with a radius of a defined curvature.

Claims 3-12: Method of forming different type of trenches.